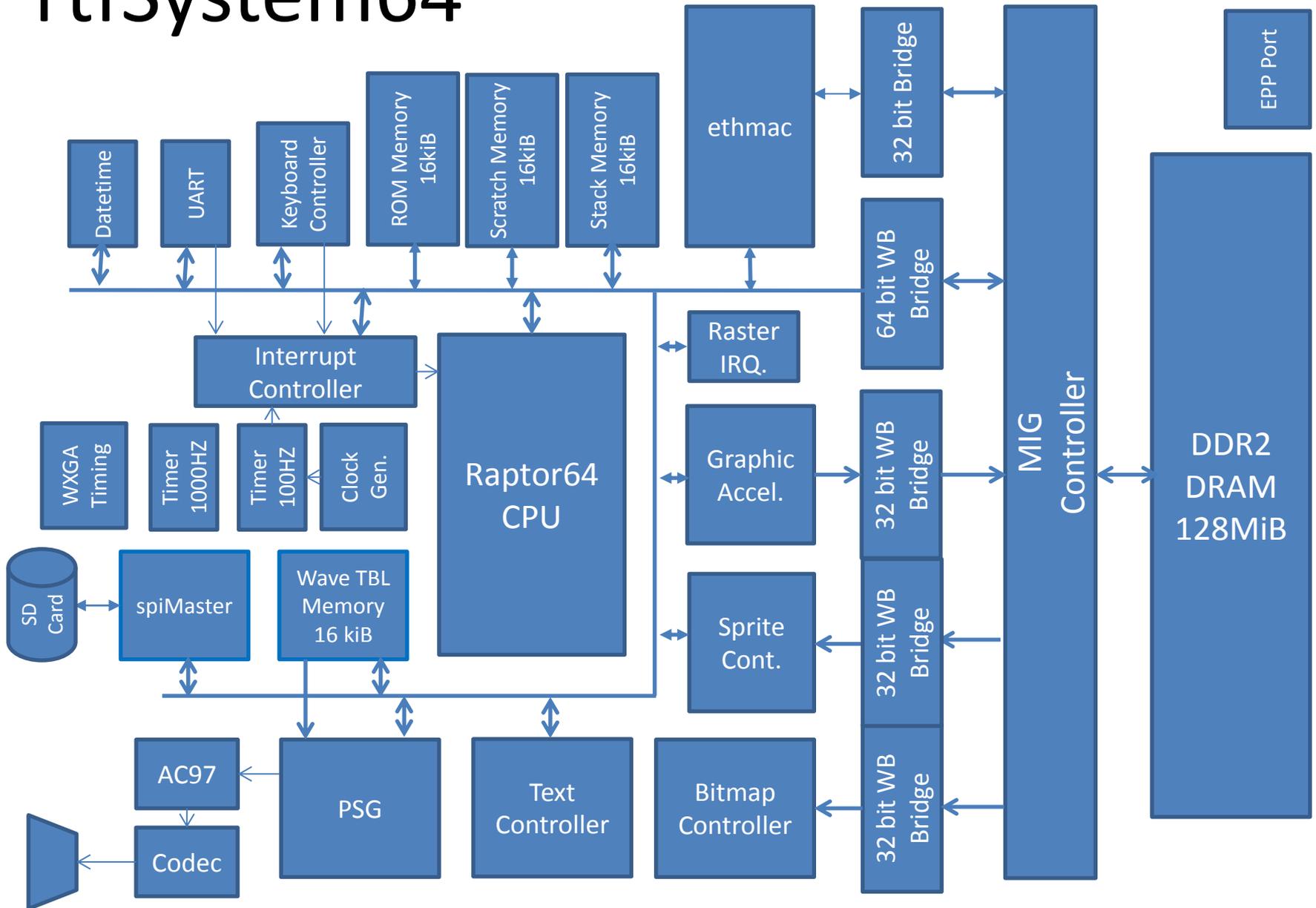


rtfSystem64



Features

- 64 bit Raptor64 CPU
- pixel plot / line draw accelerator
- 8, 256 Color sprites
- 1364x768x8bpp Bitmap screen
- 84x47 programmable text mode display
- 4 Channel ADSR sound generator with 16kB wave table
- 16 interrupt source programmable interrupt controller
- USB/PS2 keyboard interface
- Sdcard interface
- Date/time keeping

Datetime udt1

- This is a date/time keeping core. Documentation for this core is found in the 'Other' tab
- in OpenCores.

Bootrom ubr1

- This is the boot ROM for the Raptor64 processor. It is a pipelined memory for
- burst access by the processor. It has a three cycle latency, then provides data
- every cycle afterwards. The boot ROM responds to the address range \$FFFFFFFFFFFFxxxx

spiMaster uspi1

- This core is used to access the SDCard which is attached to port JB 1-6 of the Atlys
- board. This core is available elsewhere in OpenCores. Please refer to the documentation
- for that core.

sema_mem

This core provides 2048 eight bit counted semaphores for system use. The semaphores are located in the system I/O range from \$DB0000 to \$DBFFFF. Each semaphore uses a block of 16 addresses. The low order four bits of the address are used to increment or decrement the semaphore. For example if the address is \$DB0003 then the semaphore at \$DB000x is incremented or decremented by 3. The semaphore is incremented by a write cycle and decremented by a read cycle. Note that saturating counters are used – the semaphore won't decrement below zero or increment above \$FF. If low nybble is a zero then the semaphore acts like a regular memory. A write cycle will write the data on the databus to the semaphore, and a read cycle will read the semaphore's value. Note that a read cycle to non-zero addresses will both read the semaphore value and decrement it.

stkmem

Stkmem is a word wide memory used as a temporary stack memory. It only supports Full word reads and writes. This memory was used to get the processor up and running in a simple fashion prior to having the bus bridges and DDR2 RAM access available. It is Used primarily as a context startup stack area. Each context is allowed 1k. This core Responds in the address range \$FFFFFFFFFE0000 to \$FFFFFFFFFEFFFF. There are Four shadows of the 16kB core.

scratchmem

scratchmem is a word wide memory used as a scratchpad space. It supports byte sized access for reads and writes. This memory was used to get the processor up and running in a simple fashion prior to having the bus bridges and DDR2 RAM access available. It is Used primarily to contain system variables – things like the keyboard buffer are located In this memory. This core responds to the address range \$0000000000000000 to \$000000000000FFFF – there are four shadows of the 16k core.

WaveTblMem

This memory is shared between the CPU and the PSG. It is for storing audio wave data. The memory is only 12 bits wide as this is the resolution that the PSG supports. Note that it's the upper 12 bits of a 16 bit word that are used. The low order nybble is Not connected. The PSG can read this memory periodically to generate sounds based on waveforms stored in the memory. This allows the PSG to generate arbitrary waveforms.

Bus Error – ube1

This module takes care of providing a bus timeout error signal. If the system bus has been inactive for about a second, then this module activates an error signal (err_o). The err_i signal is processed by the processor, and the processor will reset the context that caused the bus error. Program code in the boot ROM does this.

Wb32toMig32 – ubridge_x

This module is instanced multiple times and acts as a bridge between WISHBONE busses used by the system, and a 32 bit MIG bus. The MIG bus is provided by the FPGA vendor. The bus bridge supports single cycle, and burst cycle bus cycles.

mig_39 u_mig_39

This core is used to interface to the DDR2 memory on the Atlys board. It is a core Generated by the vendor tools. Please see the vendors documentation for the core.

AC97

This module shadows a LM4550 AC97 controller and provides a system interface to the controller. Internally it makes use of a core provided by Digilent, the Atlys board Vendor. Please see their website for information on that core.

This module looks like it has the same register set as the LM4550 and it takes care of Updating and reading registers of the LM4550. Register port 68h is used by the module as a status register, to indicate the update status of other registers. Otherwise review the datasheet for the LM4550 to see how the AC97 controller works.

The core responds to the I/O address range of \$DC1000 to \$DC10FF.

PSG16 – u_psg

This module provides sound generation using a four channel ADSR generator. It feeds The AC97 controller with audio data. The core also shares a wave table memory with the CPU. The PSG responds to the I/O address range \$D50000 to \$D500FF. Documentation for this core can be found under the 'Other' tab in OpenCores.

rtfSimpleUart – uart

This core provides simple serial I/O. Documentation for this core can be found Under the 'Communications' tab in OpenCores. The core responds to the I/O Address range \$DC0A0x.

rtfGraphicsAccelerator

This core provides line draw and point plot / fetch acceleration. It responds to the I/O address range \$DAE0xx. This core is in initial stages of development.

Reg

00 – Pen color	this is a 24 bit register
04 – Fill Color	currently not used
08 – X0	'x' coordinate (start of line)
0C – Y0	'y' coordinate
10 – X1	'x' coordinate (end of line)
14 – Y1	'y' coordinate (end of line)
34 – pixel color	returns the color of a pixel – 24 bits
38 – state	graphics command state (read only)
3C – cmd	graphics command to execute

Supported graphics commands:

01	Draw Pixel
02	Draw line
08	Get pixel

rtfSpriteController

rtfBitmapController

This core provides a bitmapped graphics display in a 1364 x 768 x 8bpp format. Bitmapped display memory is at \$100200000. There are no programmable registers associated with the core. The core uses a WISHBONE burst master controller to interface with memory. Documentation for this core can be found under the 'Video' tab at OpenCores.org.

Ethmac – uemac1

This core is the ethmac core provided under the communications tab in OpenCores.org. Please see the documentation provided there. The core is setup to respond to the I/O address range of \$DC2xxx.

rtfTextController

This core provides a text display. It responds to the following I/O address ranges:

\$D0xxxx = text screen display memory

\$D1xxxx = text attribute display memory

\$D2xxxx = text character bitmap memory

\$DA00xx = register set

Documentation for this core can be found under the 'Video' tab at OpenCores.org

PS2KeybdToAscii

This core provides a 'cooked' interface to a PS2 style keyboard. It translates the PS2 scan codes to Ascii and also provides status for lock keys, control key, shift key, And a alt key.

Reg

00 – ascii code reg

bit 0 to 7 = ascii code (an extended set)

bit 15 = keyboard strobe indicator, when this bit is set a keyboard character has been received by the controller.

bit 8 = shift status 1 = down, 0 = up

bit 9 = control status 1 = down, 0 = up

bit 10 = alt status 1 = down, 0 = up

bit 11 = keyup / keydown status 1=keyup, 0 = keydown

bit 12 = numlock status

bit 13 = capslock status

bit 14 = scroll lock status

02 – accessing this register clears the strobe status

PS2KeybdToAscii

The keyboard interface provides an interrupt to the system. System interrupt signal #15 is used. This is the lowest priority interrupt in the system.

The keyboard interface also provides a high-priority interrupt #1 when CTRL-ALT-DEL is pressed on the keyboard.

ds1626io - utmp

This core provides an interface to a ds1626 based temperature sensor. This core is currently under development.

WXGASyncGen1366x768_60Hz u3

This core generates the WXGA sync and blanking timing. The supported format is 1366x768.

dvi_out_native u2

This core is an interface to the HDMI output. It takes a pixel clock, sync, and color Data and formats it appropriately for HDMI output. This core is provided by the FPGA vendor. Please see the vendor documentation for this core.

clkgen1366x768 – u1

This is the primary clock generating core for the system. It provides various clocks needed by the system, including system timing clock (20 MHz), DDR2 RAM clock, WXGA timing clock (85 MHz). It also provides 100Hz date/time keeping and interrupt clock, and 1000Hz Context switching clock.

DDR2 -RAM

The DDR2 RAM is clocked at 200MHz resulting in a maximum memory bandwidth of 800 MB/s. Note that the Atlys board supports a much higher memory bandwidth (800MHz data rate = 1.6GB/s) but it is not used by this system.